AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) Apparatus for processing data, said apparatus comprising:

a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain and a non-secure domain, said plurality of modes including:

at least one secure mode being a mode in said secure domain; and

at least one non-secure mode being a mode in said non-secure domain;

wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode;

said processor is responsive to one or more exception conditions for triggering exception processing; and

said processor being responsive to one or more parameters stored in a programmable exception trap mask register, said one or more parameters specifying which of said exceptions should be handled by a secure mode exception handler executing in a secure mode and which of said exceptions should be handled by an exception handler executing in a mode within a current one of said secure domain and said non-secure domain when that exception occurs.

2. Canceled.

3. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim ~~2~~1, wherein said exception trap mask register is writable when said processor is in a secure mode and said exception trap mask register is non-writable when said processor is in a non-secure mode.

4. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim ~~2~~1, further comprising a configuration controlling coprocessor associated with said processor and wherein said exception trap mask register is a register within said configuration controlling coprocessor.

5. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim 1, wherein at least one of said parameters is a signal value provided at a hardware input to said processor.

6. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim 1, wherein said secure exception handler is part of a secure operating system operable in said secure mode.

7. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim 1, wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode.

8. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim 1, wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode required for handling of an exception as specified by said parameters takes place via said monitor mode, said processor being operable at least partially in said monitor

mode to execute a monitor program to manage switching between said secure mode and said non-secure mode.

9. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim 8, wherein said monitor program may change said parameters to determine where an exception should be handled.

10. (currently amended) ~~Apparatus~~ The apparatus as claimed in claim 8, wherein said processor includes a register bank and said monitor program is operable when executed by said processor to flush at least a portion of said register bank shared between said secure mode and said non-secure mode when switching from said secure mode to said non-secure mode such that no secure data held within said register bank may pass from said secure mode to said non-secure mode other than as permitted by said monitor program.

11. (currently amended) A method of controlling exception processing of a processor~~processing data~~, said method comprising ~~the steps of~~:

executing a program with ~~a~~ said processor ~~operable~~ configured to operate in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain or a non-secure domain, said plurality of modes including:

at least one secure mode being a mode in said secure domain; and

at least one non-secure mode being a mode in said non-secure domain;

wherein when said processor is executing a program in a secure mode, said program has access to secure data which is not accessible when said processor is operating in a non-secure mode;

in response to one or more exception conditions, triggering exception processing using an exception handler;

wherein said processor selects an exception handler in response to one or more parameters stored in a programmable exception trap mask register, said one or more parameters specifying which of said exceptions should be handled by a secure mode exception handler executing in a secure mode and which of said exceptions should be handled by an exception handler executing in a mode within a current one of said secure domain and said non-secure domain when that exception occurs.

12. Canceled.

13. (currently amended) A method as claimed in claim 12~~1~~1, wherein said exception trap mask register is writable when said processor is in a secure mode and said exception trap mask register is non-writable when said processor is in a non-secure mode.

14. (currently amended) A method as claimed in claim 12~~1~~1, further comprising a configuration controlling coprocessor associated with said processor and wherein said exception trap mask register is a register within said configuration controlling coprocessor.

15. (original) A method as claimed in claim 11, wherein at least one of said parameters is a signal value provided at a hardware input to said processor.

16. (original) A method as claimed in claim 11, wherein said secure exception handler is part of a secure operating system operable in said secure mode.

17. (original) A method as claimed in claim 11, wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode.

18. (currently amended) A method as claimed in claim 11, wherein said processor is also operable in a monitor mode and any switching between a secure mode and a non-secure mode required for handling of an exception as specified by said parameters takes place via said monitor mode, said processor being ~~operable~~ at least partially in said monitor mode ~~to~~ and ~~execute~~ executing a monitor program to manage switching between said secure mode and said non-secure mode.

19. (original) A method as claimed in claim 18, wherein said monitor program may change said parameters to determine where an exception should be handled.

20. (currently amended) A method as claimed in claim 18, wherein said processor includes a register bank and said monitor program ~~is operable to flush~~ flushes at least a portion of said register bank shared between said secure mode and said non-secure mode when switching from said secure mode to said non-secure mode such that no secure data held within said register

bank may pass from said secure mode to said non-secure mode other than as permitted by said monitor program.

21. (currently amended) A computer program product having a computer program embodied in a tangible medium and executable on a data processing apparatus ~~operable~~ to control ~~a~~ said data processing apparatus in accordance with the method of claim 11.